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Computer Aided Design, 2004. ICCAD-2004. IEEE/ACM Internal
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□   **2. TPartition: testbench partitioning for hardware-accelerated f verification**
Young-Il Kim; Chong-Min Kyung;
Design & Test of Computers, IEEE
Volume 21, Issue 6, Nov-Dec 2004 Page(s):484 - 493
Digital Object Identifier 10.1109/MDT.2004.101

AbstractPlus | References | Full Text: PDF(152 KB)   **IEEE JNL**
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□   **3. Verification of transaction-level SystemC models using RTL**
Jindal, R.; Jain, K.;
Formal Methods and Models for Co-Design, 2003. MEMOCODE
First ACM and IEEE International Conference on
24-26 June 2003 Page(s):199 - 203

AbstractPlus | Full Text: PDF(213 KB)   **IEEE CNF**
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□   **4. A DSP realization of a CELP testbench**
Wong, T.; Gargour, C.; Batani, N.;
Electrical and Computer Engineering, 1993. Canadian Conferenc
14-17 Sept. 1993 Page(s):167 - 170 vol.1
Digital Object Identifier 10.1109/CCECE.1993.332209

AbstractPlus | Full Text: PDF(348 KB)   **IEEE CNF**
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□   **5. Checking temporal properties in SystemC specifications**
Braun, A.; Gerlach, J.; Rosenstiel, W.;
High-Level Design Validation and Test Workshop, 2002. Seventh
27-29 Oct. 2002 Page(s):23 - 27

AbstractPlus | Full Text: PDF(550 KB)   **IEEE CNF**
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6. **Re-useable hardware/software co-verification of IP blocks**
Bruce, A.; Goodenough, J.;
ASIC/SOC Conference, 2001. Proceedings. 14th Annual IEEE Ir
12-15 Sept. 2001 Page(s):413 - 417
Digital Object Identifier 10.1109/ASIC.2001.954737

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7. **Verification and management of a multimillion-gate embedd·**
Notbauer, J.; Albrecht, T.; Niedrist, G.; Rohringer, S.;
Design Automation Conference, 1999. Proceedings. 36th
21-25 June 1999 Page(s):425 - 428
Digital Object Identifier 10.1109/DAC.1999.781353

AbstractPlus | Full Text: PDF(372 KB)   **IEEE CNF**
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8. **Concurrent design of a chipset and its runtime environment**
ten Hagen, K.; Meyr, H.;
ASIC Conference and Exhibit, 1992., Proceedings of Fifth Annuɛ
21-25 Sept. 1992 Page(s):525 - 528
Digital Object Identifier 10.1109/ASIC.1992.270207

AbstractPlus | Full Text: PDF(340 KB)   **IEEE CNF**
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9. **A method for accelerating test environments**
Bauer, M.; Ecker, W.; Henftling, R.; Zinn, A.;
EUROMICRO Conference, 1999. Proceedings. 25th
Volume 1, 8-10 Sept. 1999 Page(s):477 - 480 vol.1
Digital Object Identifier 10.1109/EURMIC.1999.794513

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10. **Synthesis of synchronous assertions with guarded atomic ɛ**
Pellauer, M.; Lis, M.; Baltus, D.; Nikhil, R.;
Formal Methods and Models for Co-Design, 2005. MEMOCODE
Third ACM and IEEE International Conference on
11-14 July 2005 Page(s):15 - 24
Digital Object Identifier 10.1109/MEMCOD.2005.1487886

AbstractPlus | Full Text: PDF(558 KB)   **IEEE CNF**
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verification of avionics protocol controllers**
Dellacherie, S.; Burgaud, L.; di Crescenzo, P.;
Digital Avionics Systems Conference, 2003. DASC '03. The 22n
Volume 1, 12-16 Oct. 2003 Page(s):1.A.1 - 1.1-8 vol.1
Digital Object Identifier 10.1109/DASC.2003.1245801

AbstractPlus | Full Text: PDF(572 KB)   **IEEE CNF**
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12. **Instruction based testbench architecture**
Ho-seok Choi; Seung-beom Lee; Sin-chong Park;
System-on-Chip for Real-Time Applications, 2005. Proceedings.
Workshop on
20-24 July 2005 Page(s):329 - 333
Digital Object Identifier 10.1109/IWSOC.2005.76

AbstractPlus | Full Text: PDF(144 KB)   **IEEE CNF**
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☐ 13. **Automatic generation of software/hardware co-emulation in transaction-level communication**
Young-Il Kim; Ki-Yong Aim; Heejun Shim; Wooseung Yang; You Ki; Chong-Min Kyung;
VLSI Design, Automation and Test, 2005. (VLSI-TSA-DAT). 200 International Symposium on
27-29 April 2005 Page(s):196 - 199

AbstractPlus | Full Text: PDF(280 KB)   **IEEE CNF**
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☐ 14. **Qualifying precision of abstract SystemC models using the Verification Standard**
Carbognani, F.; Lennard, C.K.; Ip, C.N.; Cochrane, A.; Bates, P.
Design, Automation and Test in Europe Conference and Exhibiti
2003 Page(s):88 - 94 suppl.
Digital Object Identifier 10.1109/DATE.2003.1186677

AbstractPlus | Full Text: PDF(260 KB)   **IEEE CNF**
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☐ 15. **Robust Vera coding techniques for gate-level and tester-coi verification environments**
Litterick, M.; Geishauser, J.;
Microprocessor Test and Verification, 2004. Fifth International W
9-10 Sept. 2004 Page(s):64 - 78
Digital Object Identifier 10.1109/MTV.2004.22

AbstractPlus | Full Text: PDF(264 KB)   **IEEE CNF**
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Paplinski, A.P.; Bhattacharjee, N.; Greif, C.;
Digital Systems, Design, 2001. Proceedings. Euromicro Sympos
4-6 Sept. 2001 Page(s):254 - 261
Digital Object Identifier 10.1109/DSD.2001.952290

AbstractPlus | Full Text: PDF(536 KB)   **IEEE CNF**
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☐ 17. **Modeling and prototyping of communication systems using**
Indrusiak, L.S.; Prudencio, R.B.; Glesner, M.;
Rapid System Prototyping, 2005. (RSP 2005). The 16th IEEE In Workshop on
8-10 June 2005 Page(s):225 - 231
Digital Object Identifier 10.1109/RSP.2005.32

AbstractPlus | Full Text: PDF(296 KB)   **IEEE CNF**
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☐ 18. **Methodology and code reuse in the verification of telecomm**
Petlin, O.; Genusov, A.; Wakeman, L.;
ASIC/SOC Conference, 2000. Proceedings. 13th Annual IEEE Iı
13-16 Sept. 2000 Page(s):187 - 191
Digital Object Identifier 10.1109/ASIC.2000.880699

AbstractPlus | Full Text: PDF(424 KB)   **IEEE CNF**
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☐ 19. **Proceedings International Verilog HDL Conference and VHC Users Forum**
Verilog HDL Conference and VHDL International Users Forum, ˙

Proceedings., 1998 International
16-19 March 1998
Digital Object Identifier 10.1109/IVC.1998.660671

AbstractPlus | Full Text: PDF(180 KB)   **IEEE CNF**
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☐   **20. How to efficiently build VHDL testbenches**
Schutz, M.;
Design Automation Conference, 1995, with EURO-VHDL, Proce
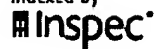'95., European
18-22 Sept. 1995 Page(s):554 - 559
Digital Object Identifier 10.1109/EURDAC.1995.527459

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